1. A radio frequency (RF) multi-antenna access point system implemented in a single chip integrated circuit chip (IC) comprising:

a baseband processor circuit located in a first portion of the single chip IC for handling data transmissions during a first operating mode in a channel between a first access point and a second access point;

a multi-antenna signal processing circuit located in a second portion of the single chip IC for handling data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to:

(a) receive M independent RF modulated input signals from said second access point;

(b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said first operating mode and said second operating mode are automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel.

2. The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit includes an analog to digital converter, and a digital to analog converter for interfacing to an antenna.

3. The RF multi-antenna access point system of claim 2, wherein said multi-antenna signal processing circuit includes a Fast Fourier Transform (FFT) Circuit.

4. The RF multi-antenna access point system of claim 3, wherein said multi-antenna signal processing circuit includes a preamble acquisition circuit for performing a preamble acquisition to align an FFT data frame with an 802.11x based data stream.

5. The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit processes at least 4 separate input signals representing a data stream multiplexed over 4 separate bit streams.

6. The RF multi-antenna access point system of claim 1, wherein said channel mixing matrix performs an operation that computes a recovered data signal x as follows:

$$x = b1*y1 + b2*y2 + x0$$

where b1 and b2 are equalization coefficients computed by said multi-antenna signal processing circuit, y1 and y2 are received data from separate baseband channels, and x0 is a recovered signal from an adjacent channel.

7. The RF multi-antenna access point system of claim 1, wherein space division multiple access is realized by separating different RF signals from different directions simultaneously in the single chip IC.

8. The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit extends a data transmission range achieved by said baseband processor circuit between said first access point and said second access point.

9. The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit increases a data transmission rate achieved by said baseband processor circuit between said first access point and said second access point.

10. The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit transmits M separate data signals to said second access point.

11. The RF multi-antenna access point system of claim 10, wherein a localized encryption is achieved for said second access point by independently controlling said M separate transmission signals.

12. The RF multi-antenna access point system of claim 1, wherein said first access point can be configured during a data transmission to transmit with an energy level which is substantially the same as a noise level to locations other than a localized region where said second access point is located.

13. An 802.11x compatible radio frequency (RF) multi-antenna access point enhancement circuit implemented in a single chip integrated circuit (IC) comprising:

a multi-antenna signal processing circuit situated in a first portion of the single chip IC and configured as a first access point adapted to:

(a) operate simultaneously with a first baseband processor situated in a second portion of the single chip IC, so that said first baseband processor handles data transmissions in a first mode between said first access point in accordance with an 802.11x protocol, and a second access point under a first channel transmission condition, and said multi-antenna signal processor handles data transmissions in a second mode between said first access point and said second access point in accordance with an 802.11x protocol under a second channel transmission condition;

(b) receive M independent RF modulated input signals from said second access point when the second channel transmission mode exists between the first access point and said second access point;

(c) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

(d) transmit an RF modulated signal to said second access point using a point coordination function (PCF) mode associated with said 802.11x protocol so as to maintain timing compatibility;

wherein said multi-antenna signal processing circuit operates with a first baseband processor to receive and transmit RF signals in a channel between said first access point and said second access point.

14. The circuit of claim 13 wherein said multi-antenna signal processing circuit processes data using a high rate direct sequence spread spectrum (HR/DSSS) physical layer frame structure that has a preamble and header compatible with said 802.11x protocol.

15. The circuit of claim 13, wherein said header includes additional data to identify a high rate mode.

16. The circuit of claim 13, wherein said header includes additional data to identify a modulation format.

17. The circuit of claim 13, wherein said first baseband processor sends multicast transmissions to a first set of targets within a first range of said first access point, and said multi-antenna signal processing circuit sends multicast transmissions to a second set of targets within a second range of said first access point.

18. The circuit of claim 13, wherein first baseband processor communicates with a first set of targets during a first access period, and said multi-antenna signal processing circuit communicates with a second set of targets during a second access period.

19. The circuit of claim 18, wherein said first access period and said second access period are alternated at a predetermined ratio.

20. The circuit of claim 13, wherein said multi-antenna signal processing circuit uses a wave beam transmission to communicate selectively to a target in a specific location, and not to other targets.

21. The circuit of claim 13, wherein said multi-antenna signal processing circuit is incorporated as part of a closed circuit television monitoring system, and said M independent signals are transmitted by N individual cameras.

22. The circuit of claim 13, wherein a receive sensitivity of said first access point can be improved by selectively adding additional multi-antenna signal processing circuit modules for a data transmission, and/or increasing M.

23. A single chip integrated circuit (IC) radio frequency (RF) multi-antenna access point circuit comprising:

a baseband processor circuit in the single chip IC for handling data transmissions during a first operating mode in a channel between a first access point and a second access point;

a multi-antenna signal processing circuit in the single chip IC for handling data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to:

(a) receive M independent RF modulated input signals from said second access point;

(b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said first operating mode and said second operating mode are automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel;

a modulator/demodulator circuit in the single chip IC coupled to an antenna assembly and said multi-antenna signal processing circuit and baseband processor circuit for extracting I/Q data samples from an RF modulated received signal;

a media access controller in the single chip IC coupled to said multi-antenna signal processing circuit and baseband processor circuit for interfacing to a host computing system.